REMARKS

Section 3 of the Office Action

Claims 1-4, 6-14, 17-21, and 26-28 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-10, 13-33, and 36-46 of US Application No. 10/059,588, published as US 2003/0141507. Applicants respectfully traverse the rejection. Claim 1 is amended to recite "a portion of the p-type region proximate the metal reflector is uninterrupted by the photonic crystal structure." This amendment is supported by, for example, Figs. 2 and 13 and accompanying text. Applicants have found no such teaching or suggestion in the claims of US 2003/0141507, which Applicants note has since issued as US 7,279,718.

Section 4 of the Office Action

Claims 1, 2, 4, and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Gopinath, US 2002/0079497. Applicants respectfully traverse the rejection. Claim 1 recites "a metal reflector disposed . . . on at least a portion of a surface of the p-type region opposite the active region; and . . . a portion of the p-type region proximate the metal reflector is uninterrupted by the photonic crystal structure." Thus, a portion of the p-type material must be BOTH between the metal reflector and the active region AND uninterrupted by the photonic crystal structure. The Examiner does not specify what structure in Gopinath is a p-type region. However, Applicants respectfully note that ALL of the semiconductor material between either of upper and lower mirror stacks 12 and 22 and quantum wells 20 are interrupted by pillars 30/regions 32. Accordingly, Gopinath fails to teach every element of claim 1. Claims 2, 4, 13, and 14 depend from claim 1 and are therefore allowable over Gopinath for at least the same reason as claim 1.

Sections 5 and 6 of the Office Action

PATENT LAW GROUP LLP
2635 N. FIRST ST.
SUITE 223
SAN JOSE, CA 95134
(408) 382-0480
FAX (408) 382-0481

Claims 1, 2, 4, 8, 13, 14, 17-21, 26, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Erchak et al., US 6,831,302 (hereinafter "Erchak"). Claims 3, 5-7, 9-12, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erchak. Applicants intend to submit an appropriate declaration to establish invention of the subject matter of any rejected claim prior to the effective date of Erchak, once the other prior art rejections made by the Examiner are overcome.

Section 7 of the Office Action

Claims 1, 2, 4, 13, 14, 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lester, U.S. Patent 6,091,085 in view of Scherer et al., U.S. Patent 6,534,798 (hereinafter "Scherer"). Applicants respectfully traverse the rejection.

In a previous response, Applicants pointed out that the only possible major surface of Lester's semiconductor structure available for Scherer's reflector is the top surface, since the bottom surface cannot be accessed due to substrate 33. Applicants noted a person of skill in the art would never be motivated to form both Lester's light pipes and a reflector on the top surface of a semiconductor device, since the light pipes and the reflector serve opposite purposes: the light pipes extract light through the top surface, while the reflector prevents light from escaping through the top surface. As these effects cancel each other out, a person of skill in the art would not expect such a device to have high light output, as promised by the Examiner.

In response, the Examiner states on page 8 "it would have been obvious to one of ordinary skill in the art . . . to form the '085 reference's light emitting device such that it includes a metal reflector such as the silver reflector 18, taught by Scherer, disposed on at least a portion of a surface of the p-type region (at the lower surface of the p-n junction 32, Fig. 7, the '085 reference)." The Examiner thus proposes putting Scherer's metal reflector between Lester's sapphire substrate and III-nitride layers.

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SUITE 223
SAN JOSE, CA. 95134
(408) 382-0480
FAX (408) 382-0481

Applicants respectfully submit that there is no expectation that such a combination can be successfully made. Scherer teaches, at column 5 line 18 et seq. "membrane 12 is removed from its [GaAs] substrate [14] by dissolving sacrificial AlAs layer 16. . . . The lifted-off membrane 12 . . . with thick silver layer 18 on top is then Van der Waals bonded onto a silver coated silicon wafer 20." Chemical etching of GaAs substrates is well known and easy to accomplish. In contrast, a person of skill in the art would understand that removing Lester's sapphire substrate with Scherer's etch is impossible. In addition, even if it were possible to remove Lester's sapphire substrate by Scherer's etch, a person of skill in the art would expect Lester's III-nitride layers to be highly damaged, likely destroyed, by the type of transfer taught by Scherer. Accordingly, there is no expectation that Lester can be successfully combined with Scherer. Claim 1 is thus allowable over the combination of Lester and Scherer. Claims 2, 4, 13, 14, 21 and 26 depend from claim 1 and are thus allowable over Lester and Scherer for at least the same reasons as claim 1.

Section 8 of the Office Action

Claims 1-28, 32, 33, and 38 are rejected under 35 U.S.C. 103(a) as obvious over Scherer in view of Lester. Applicants respectfully traverse the rejection.

The Examiner states on page 9 of the office action:

> [Scherer] does not disclose forming a photonic crystal structure in at least a portion of the n-type region and in a portion of the doped III-nitride light emitting layer and as claimed.
>
> . . .
>
> [I]t would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '798 reference's device such that a photonic structure formed at least in a portion of the n-type region (or the p-type region) and in a portion of the doped III-nitride light emitting layer, in place of or in addition to microcavities in the metallic layer.

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2635 N. FIRST ST.
SUITE 223
SAN JOSE, CA 95134
(408) 382-0480
FAX (408) 382-0481

As noted above, a person of skill in the art would appreciate that III-nitride material cannot be readily substituted for the GaAs-based material of Scherer's device, because

suitable III-nitride material cannot be grown on GaAs substrates, commonly used III-nitride substrates cannot be readily etched away by the process proposed by Scherer, and III-nitride crystals are likely to be damaged by the transfer process taught by Scherer.

In addition, as pointed out in a previous office action, Scherer **teaches away** from combination with Lester at column 4, line 36, which states "[t]he increased light emission is due to an increase in the efficiency and an increase in the pumping intensity resulting from trapping of pump photons within the microcavity." Emphasis added. This passage teaches that it is preferred to trap photons within the microcavity, not extract them as with Lester's light pipes. The passage suggests that including a structure like Lester's that directs light to the surface of the device would actually result in WORSE performance, rather than better as suggested by the Examiner. **The Examiner has ignored this argument,** stating only in his response to arguments that "one of ordinary skill in the art clearly see [sic] the benefits of combing [sic] the references, as detailed above in paragraph numbered 8 for the purpose of increasing light outputs over or in addition to an increased light output."

Since Scherer cannot be successfully combined with Lester and since Scherer teaches away from combination with Lester, claim 1 is allowable over Scherer and Lester. Claims 2-28, 32, and 33 depend from claim 1 and are therefore allowable over Scherer and Lester for at least the same reasons as claim 1.

Section 9 of the Office Action

Claims 1-16, 21, 26-28, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joannopoulos et al., US 5,955,749 "in view of availability of III-nitride semiconducting material." See Office Action, page 10. Applicants respectfully traverse the rejection.

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SAN JOSE, CA. 95134
(408) 382-0480
FAX (408) 382-0481

First, as described above in reference to Scherer and Lester, III-nitride layers cannot be readily transferred from a growth substrate to a metal layer as proposed by the Examiner.

Neither Joannopoulos nor the "availability of III-nitride semiconductor material" teach or suggest how to form the device proposed by the Examiner. Second, the Examiner has pointed to no teaching in Joannopoulos of "a contact disposed on a top side of the III-nitride semiconductor structure" as recited in claim 1.

Since the combination of Joannopoulos with "availability of III-nitride semiconducting material" does not teach all the elements of claim 1, and since Joannopoulos cannot be modified as proposed by the Examiner, claim 1 is allowable over the Examiner's analysis of Joannopoulos. Claims 2-16, 21, 26-28, 32, and 33 depend from claim 1 and are therefore allowable over Joannopoulos for at least the same reason as claim 1.

In view of the above arguments, Applicants respectfully request allowance of all pending claims. Should the Examiner have any questions, the Examiner is invited to call the undersigned at (408) 382-0480.

Respectfully submitted,

/Rachel V. Leiterman/

Rachel V. Leiterman
Attorney for Applicants
Reg. No. 46,868

PATENT LAW
GROUP LLP
2635 N. FIRST ST
SUITE 223
SAN JOSE, CA 95134
(408) 382-0480
FAX (408) 382-0481